WHAT IS CLAIMED IS:

1. A decoder for a memory device, comprising:

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein each of the logic cells includes a floating gate transistor includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

2. The decoder of claim 1, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

3. The decoder of claim 1, wherein the low tunnel barrier intergate insulator includes a transition metal oxide.

4. The decoder of claim 3, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

5. The decoder of claim 1, wherein the low tunnel barrier intergate insulator includes a Perovskite oxide tunnel barrier.

6. The decoder of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

7. The decoder of claim 6, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

8. The decoder of claim 1, wherein at least one of the output lines includes a redundant wordline.

9. A decoder for a memory device, comprising:

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein each of the logic cells includes a vertical non-volatile memory cell including:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

10. The decoder of claim 9, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

11. The decoder of claim 9, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

12. The decoder of claim 11, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

13. The decoder of claim 9, wherein the floating gate includes a vertical floating gate formed alongside of the body region.

14. The decoder of claim 13, wherein the control gate includes a vertical control gate formed alongside of the vertical floating gate.

15. The decoder of claim 9, wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region.

16. The decoder of claim 15, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

17. A programmable decode circuit for a semiconductor memory, comprising:

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein each of the logic cells includes a vertical non-volatile memory cell including:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the metal layer;

a second metal layer formed on the metal oxide intergate insulator; and

a polysilicon control gate formed on the second metal layer.

18. The programmable decode circuit of claim 17, wherein first and the second metal layers are lead and the metal oxide intergate insulator is lead oxide (PbO).

19. The programmable decode circuit of claim 17, wherein the first and second metal layer are aluminum and the metal oxide intergate insulator is aluminum oxide (Al_2O_3).

20. The programmable decode circuit of claim 17, wherein the first and the second metal layers include transition metal layers and the metal oxide intergate insulator includes a transition metal oxide intergate insulator.

21. The programmable decode circuit of claim 20, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

22. The programmable decode circuit of claim 17, wherein the metal oxide intergate insulator includes a Perovskite oxide intergate insulator.

23. The programmable decode circuit of claim 17, wherein the floating gate transistor includes a vertical floating gate transistor.

24. The programmable decode circuit of claim 17, wherein each input line is integrally formed with the polysilicon control gate for addressing the floating gate.

25. The programmable decode circuit of claim 17, wherein each input line is integrally formed with the polysilicon control gate in a trench opposing the floating gate.

26. The programmable decode circuit of claim 17, wherein the programmable logic array includes a number of buried source lines which are formed integrally with the first source/drain region and are separated from the semiconductor substrate by an oxide layer.

27. The programmable decode circuit of claim 17, wherein each address line includes a vertically oriented address line having a vertical length of less than 50 nanometers.

28. A decode circuit for a semiconductor memory, comprising:
a number of address lines;
a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein each of the logic cells includes a vertical non-volatile memory cell including:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a plurality of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain region of pillars in the array; and

wherein each of the number of address lines is disposed between rows of the pillars and integrally formed with the number of control gates and opposing the floating gates of the vertical non-volatile memory cells for serving as a control gate and are separated from the number of floating gates by a low tunnel barrier integrate insulator.

29. The decode circuit of claim 28, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

30. The decode circuit of claim 28, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

31. The decode circuit of claim 28, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

32. The decode circuit of claim 28, wherein the number of floating gates includes vertical floating gates formed alongside of the body region.

33. The decode circuit of claim 32, wherein the number of control gates includes vertical control gates formed alongside of the vertical floating gates.

34. The decode circuit of claim 28, wherein the number of floating gates includes horizontally oriented floating gates formed alongside of the body regions.

35. The decode circuit of claim 28, wherein the number of buried source lines are formed integrally with the first source/drain regions and are separated from the substrate by an oxide layer.

36. A memory address decoder, comprising:

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein each of the logic cells includes a vertical non-volatile memory cell including:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates, wherein the number of control gates are separated from the number of floating gates by a low tunnel barrier integrate insulator; and

a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

37. The memory address decoder of claim 36, wherein the number of address lines are disposed in a trench between rows of the pillars and oppose the floating gates of the vertical non-volatile memory cells for serving as control gates, and wherein the number of output lines couple to the second source/drain region in columns of pillars for implementing a logic function in the memory address decoder.

38. The memory address decoder of claim 36, wherein the number of address lines includes a number of complementary address lines that are disposed in a trench between rows of the pillars and oppose the floating gates of the vertical non-volatile memory cells for serving as control gates.

39. The memory address decoder of claim 36, wherein column adjacent pillars are separated by a trench and each trench includes a pair of floating gates opposing the body regions on opposite sides of the trench.

40. The memory address decoder of claim 39, wherein each trench includes a single vertically oriented address line formed between the pair of floating gates for serving as a shared control gate.

41. The memory address decoder of claim 39, wherein each trench includes a pair of vertically oriented address lines formed between the pair of floating gates, and wherein each one of the pair of vertically oriented address lines independently addresses the floating gates on opposing sides of the trench, and wherein the pair of vertically oriented address lines are separated by an insulator layer.

42. The memory address decoder of claim 39, wherein the number of address lines are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single address line.

43. The memory address decoder of claim 39, wherein the number of address lines are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of address lines.

44. The memory address decoder of claim 36, wherein column adjacent pillars are separated by a trench and each trench includes a horizontally oriented floating gate formed below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in column adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 50 nanometers opposing the body regions of the pillars.

45. The memory address decoder of claim 44, wherein the number of address lines are disposed vertically above the floating gates.

46. A memory device, comprising:

an array of wordlines and complementary bit line pairs;

a number of memory cells that are each addressably coupled at intersections of a word line with a bit line of a complementary bit line pair;

a row decoder that is coupled to the wordlines so as to implement a logic function that selects one of the wordlines responsive to an address provided to the row decoder on a number of first address lines;

a number of sense amplifiers, each coupled to a complementary pair of bit lines;

a column decoder that is coupled to the sense amplifiers so as to implement a logic function that selects one of the complementary pairs of bit lines responsive to an address provided to the column decoder on a number of second address lines; and

wherein the row decoder comprises an array of vertical non-volatile floating gate transistors that are selectively coupled to implement a logic function that selects a wordline based on addresses supplied on the number of first address lines, wherein each vertical non-volatile floating gate transistor includes;

a pillar extending outwardly from a substrate, wherein the pillar includes a first source/drain region, a body region, and a second source/drain region;

a floating gate opposing the body region in the pillar and separated therefrom by a gate oxide;

a control gate opposing the floating gates, wherein the control gate is separated from the floating gate by a low tunnel barrier integrate insulator.

47. The memory device of claim 46, wherein each of the first address lines are formed in a trench opposing the floating gates, and wherein each of the first address lines include vertically oriented address lines having a vertical length of less than 50 nanometers.

48. The memory device of claim 46, wherein each of the first address lines include horizontally oriented address lines formed above the floating gates.

49. The memory device of claim 46, wherein each of the wordlines couples to the second source/drain region of the non-volatile floating gate transistors in the row decoder.

50. The memory device of claim 46, wherein the column decoder includes an array of vertical non-volatile floating gate transistors that are selectively coupled to implement a logic function that selects one of the complementary pairs of bit lines responsive to addresses provided to the column decoder on the number of second address lines, wherein each vertical non-volatile floating gate transistor includes:

a pillar extending outwardly from a substrate, wherein the pillar includes a first source/drain region, a body region, and a second source/drain region;

a floating gate opposing the body region in the pillar and separated therefrom by a gate oxide;

a control gate opposing the floating gates, wherein the control gate is separated from the floating gate by a low tunnel barrier integrate insulator.

51. The memory device of claim 50, wherein the complementary pairs of bit lines couple to the second source/drain regions of the vertical non-volatile floating gate transistors in the column row decoder.

52. An electronic system, comprising:

a processor; and

a memory device coupled to processor, wherein the memory device includes a programmable decoder comprising:

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein each of the logic cells includes a vertical non-volatile memory cell including;

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

53. The electronic system of claim 52, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

54. The electronic system of claim 52, wherein the low tunnel barrier intergate insulator includes a transition metal oxide.

55. The electronic system of claim 54, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

56. The electronic system of claim 52, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

57. The electronic system of claim 56, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

58. The electronic system of claim 52, wherein at least one of the output lines includes a redundant wordline.

59. An electronic system, comprising:

a processor; and

a memory device coupled to processor, wherein the memory device includes a programmable decoder comprising:

a number of address lines;

a number of output lines;

wherein the address lines, and the output lines form an array;

a number of logic cells formed at the intersections of output lines and address lines, wherein each of the logic cells includes a vertical non-volatile memory cell including:

a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates, wherein the number of control gates are separated from the number of floating gates by a low tunnel barrier integrate insulator;

a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

60. The electronic system of claim 59, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

61. The electronic system of claim 59, wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

62. The electronic system of claim 61, wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

63. The electronic system of claim 59, wherein each floating gate is a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

64. The electronic system of claim 63, wherein the number of control gates are formed in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

65. The electronic system of claim 63, wherein the number of control gates are formed in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gate lines each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

66. The electronic system of claim 63, wherein the number of control gates are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate.

67. The electronic system of claim 63, wherein the number of control gates are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates.

68. The electronic system of claim 59, wherein each floating gate is a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

69. The electronic system of claim 68, wherein the number of control gates are disposed vertically above the floating gates.

70. A method of forming a logic array for a programmable decoder, the method comprising:

forming a number of address lines;

forming a number of output lines;

wherein forming the address lines, and the output lines includes forming an array;

forming a number of logic cells at the intersections of output lines and address lines, wherein forming each of the logic cells includes forming a vertical non-volatile memory cell including;

forming a first source/drain region and a second source/drain region separated by a channel region in a substrate;

forming a floating gate opposing the channel region and separated therefrom by a gate oxide;

forming a control gate opposing the floating gate; and

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate.

71. The method of claim 70, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

72. The method of claim 70, wherein forming the low tunnel barrier intergate insulator includes forming a transition metal oxide insulator.

73. The method of claim 72, wherein forming the transition metal oxide insulator includes forming the transition metal oxide insulator selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

74. The method of claim 70, wherein forming the floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

75. The method of claim 74, wherein forming the control gate includes a forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

76. The method of claim 70, wherein at least one of the output lines includes a redundant wordline.

77. A method for forming an in service programmable logic array, comprising:

forming a plurality of address lines;

forming a plurality of output lines, wherein the plurality of output and address lines form an array; and

forming a number of logic cells at the intersections of the output and address lines, wherein forming a number of logic cells includes forming a number of vertical non-volatile memory cells including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates opposing the floating gates; and

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

78. The method of claim 77, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

79. The method of claim 77, wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

80. The method of claim 77, wherein forming each control gate includes forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

81. The method of claim 77, wherein forming each floating gate includes forming a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

82. The method of claim 81, wherein forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

83. The method of claim 81, wherein forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gates each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gates are separated by an insulator layer.

84. The method of claim 81, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate.

85. The method of claim 81, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates.

86. The method of claim 77, wherein forming each floating gate includes forming a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

87. The method of claim 86, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates.

88. A method for operating an in-server programmable logic array, comprising:

writing to one or more floating gates of a number of non-volatile memory cells in one or more arrays using channel hot electron injection, wherein the non-volatile memory cells in the one or more arrays are formed at the intersections of a number of address lines and a number of output lines, wherein each non-volatile memory cell includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

erasing charge from one or more floating gates by tunneling electrons off of the floating gate and onto the control gate.

89. The method of claim 87, wherein erasing charge from one or more floating gates by tunneling electrons off of the floating gates and onto the control gates further includes:

providing a negative voltage to a substrate of an addressed cell; and

providing a large positive voltage to the control gate of the addressed cell.

90. The method of claim 87, wherein the method further includes writing to one or more floating gates by tunneling electrons from the control gate to the floating gate in one or more addressed cells.

91. The method of claim 90, wherein writing to one or more floating gates by tunneling electrons from the control gate to the floating gate in one or more addressed cells further includes:

applying a positive voltage to a substrate of an addressed cell; and

applying a large negative voltage to the control gate of the addressed cell.

92. The method of claim 88, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator.

93. The method of claim 92, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier

intergate insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

94. The method of claim 92, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from a metal layer formed on the floating gate in contact with the low tunnel barrier intergate insulator to a metal layer formed on the control gate and also in contact with the low tunnel barrier intergate insulator.

95. A method for operating an in-server programmable logic array, comprising:

writing to one or more floating gates of a number of non-volatile memory cells in one or more arrays using channel hot electron injection, wherein the non-volatile memory cells in the one or more arrays are formed at the intersections of a number of address lines and a number of output lines, wherein each non-volatile memory cell includes:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of non–volatile memory cells;

a number of address lines formed integrally with the number of control gates along a second selected direction in the array of non–volatile memory cells, wherein the number of control

gates lines are separated from the floating gates by a low tunnel barrier intergate insulator; and

a number of output lines coupled to the second source/drain regions along a third selected direction in the array of non–volatile memory cells; and

erasing charge from the one or more floating gates by tunneling electrons off of the one or more floating gates and onto the number of control gates.

96. The method of claim 95, wherein erasing charge from the one or more floating gates by tunneling electrons off of the floating gate and onto the number of control gate further includes:

providing a negative voltage to a substrate of one or more non-volatile memory cells; and

providing a large positive voltage to the control gate for the one or more non-volatile memory cells.

97. The method of claim 96, wherein the method further includes erasing an entire row of non-volatile memory cells by providing a negative voltage to all of the substrates along an entire row of non-volatile memory cells and providing a large positive voltage to all of the control gates along the entire row of non-volatile memory cells.

98. The method of claim 96, wherein the method further includes erasing an entire block of non-volatile memory cells by providing a negative voltage to all of the substrates along multiple rows of non-volatile memory cells and providing a large positive voltage to all of the control gates along the multiple rows of non-volatile memory cells.